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# DEVICE AND METHOD FOR REPAIRING A SEMICONDUCTOR MEMORY

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# DEVICE AND METHOD FOR REPAIRING A SEMICONDUCTOR MEMORY

## CROSS-REFERENCE TO RELATED APPLICATIONS

**[0001]** This is a continuation-in-part (CIP) application of U.S. Patent Application Serial No. 09/796,080, filed February 28, 2001, pending, which is a continuation of U.S. Patent Application Serial No. 09/143,283, filed August 28, 1998, issued March 6, 2001, as U.S. Patent No. 6,199,177 B1.

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## TECHNICAL FIELD

**[0002]** This invention relates in general to memory cell redundancy in semiconductor memories and, more particularly, to devices and methods for repairing semiconductor memories by replacing memory blocks that contain failing memory cells with redundant rows or columns of cells.

## BACKGROUND OF THE INVENTION

**[0003]** Semiconductor memories generally include a multitude of memory cells arranged in rows and columns. Each memory cell is capable of storing digital information in the form of a "1" or a "0" bit. To write (*i.e.*, store) a bit into a memory cell, a binary memory address having portions identifying the cell's row (the "row address") and column (the "column address") is provided to addressing circuitry in the semiconductor memory to activate the cell, and the bit is then supplied to the cell. Similarly, to read (*i.e.*, retrieve) a bit from a memory cell, the cell is again activated using the cell's memory address, and the bit is then output from the cell.

**[0004]** Semiconductor memories are typically tested after they are fabricated to determine if they contain any failing memory cells (*i.e.*, cells to which bits cannot be dependably written or from which bits cannot be dependably read). Generally, when a semiconductor memory is found to contain failing memory cells, an attempt is made to repair the memory by replacing the failing memory cells with redundant memory cells provided in redundant rows or columns in the memory.

**[0005]** Conventionally, when a redundant row is used to repair a semiconductor memory containing a failing memory cell, the failing cell's row address is permanently stored (typically in pre-decoded form) on a chip on which the semiconductor memory is fabricated by programming a non-volatile element (*e.g.*, a group of fuses, anti-fuses, or FLASH memory cells) on the chip. Then, during normal operation of the semiconductor memory, if the memory's addressing circuitry receives a memory address including a row address that corresponds to the row address stored on the chip, redundant circuitry in the memory causes a redundant memory cell in the redundant row to be accessed instead of the memory cell identified by the received memory address. Since every memory cell in the failing cell's row has the same row address, every cell in the failing cell's row, both operative and failing, is replaced by a redundant memory cell in the redundant row.

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**[0006]** Similarly, when a redundant column is used to repair the semiconductor memory, the failing cell's column address is permanently stored (typically in pre-decoded form) on the chip by programming a non-volatile element on the chip. Then, during normal operation of the semiconductor memory, if the memory's addressing circuitry receives a memory address including a column address that corresponds to the column address stored on the chip, redundant circuitry in the memory causes a redundant memory cell in the redundant column to be accessed instead of the memory cell identified by the received memory address. Since every memory cell in the failing cell's column has the same column address, every cell in the failing cell's column, both operative and failing, is replaced by a redundant memory cell in the redundant column.

**[0007]** Thus, for example, as shown in FIG. 1, a semiconductor memory 20 having failing memory cells 22, 24, 26, 28, 30, 32, 34, and 36 is repaired in the conventional manner described above using redundant rows 38, 40, and 42 and redundant columns 44, 46, and 48. As described above, the memory 20 is repaired by replacing all memory cells in columns 50, 52, and 54, including failing memory cells 22, 24, 26, and 28, with redundant memory cells in redundant columns 44, 46, and 48. Further repairs to the memory 20 are accomplished by replacing all memory cells in rows 56, 58, and 60, including failing memory cells 30, 32, 34, and 36, with redundant memory cells in redundant rows 38, 40, and 42. The process described above for repairing a semiconductor memory using redundant rows and columns is well known in the art, and is described in various forms in U.S. Patent Nos. 4,459,685, 4,601,019, 5,422,850, and 5,528,539.

**[0008]** Unfortunately, it is difficult to provide enough redundant rows or columns in a semiconductor memory to repair all failing memory cells therein using the conventional repair process described above without using an excessive amount of space (commonly known as "real estate") in the memory for the redundant rows or columns. With the increasing size of semiconductor memories continuously increasing the need for redundancy, memory designers find themselves caught between providing sufficient redundancy to successfully repair most memories and, as a result, using excessive space in the memories, or providing insufficient redundancy to save space in the memories and, as a result, having to discard memories that are unrepairable. Obviously, neither alternative is desirable.

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**[0009]** U.S. Patent No. 5,548,225 to Rountree et al. discloses a repair system that, in contrast to the conventional repair system described above, does not use an entire redundant row or column to repair each defective memory cell in a semiconductor memory. In the Rountree repair system, the column address of a defective memory cell is stored using fuses in the same manner as described above. In addition, though, a partial row address common to a group of cells in the defective cell's column that includes the defective cell itself is also stored using fuses. When a memory address is received having column and row addresses that match the stored column address and stored partial row address, a redundant memory cell in a spare column is accessed. As a result, all of the cells in the group identified by the stored column address and stored partial row address are replaced by redundant cells in the spare column, while those cells in the defective cell's column not in the identified group are not replaced. Thus, the efficiency of repairs is increased by the Rountree system because only some of the redundant cells in the spare column are used to repair the defective cell, while other redundant cells remain in the spare column to repair other defective cells.

**[0010]** Unfortunately, the Rountree repair system can be problematic as well, because storing a full column address and a partial row address for every defective memory cell in need of repair requires a great deal of storage space (*e.g.*, fuses, etc.). Consequently, the ever-increasing size of modern semiconductor memories, and the corresponding increase in the number of defective memory cells typically found, makes the Rountree repair system increasingly prohibitive to use because of the amount of storage space it requires.

**[0011]** Therefore, there is a need in the art for an improved device and method for repairing a semiconductor memory containing a failing memory cell. Such a device and method should replace the failing cell with a redundant memory cell without replacing the failing cell's entire row or column with the redundant cell's entire row or column. The device should also replace multiple failing cells in different rows or columns with redundant memory cells in a single redundant row or column in order to make more efficient use of redundant rows and columns, and should do so without the excessive need for storage space characteristic of the Rountree repair system.

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## SUMMARY OF THE INVENTION

**[0012]** A block repair device in accordance with the present invention is used in a semiconductor memory, such as a Static Random Access Memory (SRAM), having an array with a redundant row. The block repair device includes a set of non-volatile elements, such as fuses, anti-fuses, or flash EEPROM cells, that store a block repair configuration that determines the dimensions (*e.g.*, the number of rows and columns spanned) of the repair block used to repair the defective cell. Routing circuitry, such as multiplexer (mux) circuitry, in the block repair device is configured by the block repair configuration to output some received row and column address bits in a selected ratio. Comparison circuitry in the block repair device then compares the row and column address bits output by the routing circuitry with a stored portion of the address of the defective cell that defines the repair block. When a match occurs, the comparison circuitry implements a block repair by activating the redundant row and by causing data to be written to or read from the activated redundant row instead of the primary array.

**[0013]** The present invention thus provides an efficient device for implementing block repairs in a semiconductor memory. The device requires relatively few fuses or other non-volatile elements to implement a repair, in contrast to the Rountree and other conventional methods described above.

**[0014]** In other embodiments of the invention, the block repair device described above is incorporated into a semiconductor memory, a semiconductor substrate such as a wafer, a SRAM, and an electronic system.

**[0015]** In a block repair method according to the present invention, a semiconductor memory having a primary array with a defective cell and a redundant row is repaired using a block repair. The dimensions of a repair block within the primary array for repairing the defective cell are first selected, and those row and column address bits of the defective cell that define the selected dimensions of the repair block are then stored using, for example, non-volatile elements within the semiconductor memory. A block repair configuration that corresponds to the selected dimensions of the repair block is also stored using, for example, non-volatile elements. Those received row and column address bits necessary to determine whether a received address falls within the repair block are then routed in accordance with the stored block repair configuration for comparison with the stored row and column address bits of the defective cell. When a match occurs, data is then written to, or read from, a cell within the redundant row selected in accordance with non-stored row and column address bits of the defective cell.

## BRIEF DESCRIPTION OF THE DRAWING FIGURES

**[0016]** In the drawings, which illustrate what is currently regarded as the best mode for carrying out the invention and in which like reference numerals refer to like parts in different views or embodiments:

**[0017]** FIG. 1 is a prior art diagram illustrating conventional row and column redundancy in a semiconductor memory.

**[0018]** FIG. 2 is a diagram illustrating repair of a semiconductor memory in accordance with the present invention.

**[0019]** FIG. 3 is a block diagram showing a semiconductor memory in accordance with the present invention.

**[0020]** FIGS. 4A, 4B, and 4C are circuit schematics showing fuses, anti-fuses, and flash EEPROM cells capable of use as non-volatile elements in the semiconductor memory of FIG. 3.

**[0021]** FIG. 5 is a circuit schematic showing select circuitry of the semiconductor memory of FIG. 3 in more detail.

**[0022]** FIG. 6 is a circuit schematic showing mux circuitry of the semiconductor memory of FIG. 3 in more detail.

**[0023]** FIG. 7 is a diagram illustrating a semiconductor wafer on which the semiconductor memory of FIG. 3 is fabricated.

**[0024]** FIG. 8 is a block diagram of an electronic system incorporating the semiconductor memory of FIG. 3.

## DETAILED DESCRIPTION OF THE INVENTION

**[0025]** Some general characteristics of the present invention will be described with respect to FIG. 2. This description will be followed by a detailed description of various embodiments of the present invention in connection with FIGS. 3-8.

**[0026]** As shown in FIG. 2, a semiconductor memory 70 is repaired in accordance with the present invention by replacing memory blocks 72 and 74 with respective redundant rows 76 and 78. The position and dimensions (*i.e.*, number of rows and columns spanned) of the blocks 72 and 74 are adjustable so an optimum number of defective memory cells 80 may be repaired using a minimum number of redundant rows. As a result, the present invention provides a highly efficient device and method for repairing a semiconductor memory. Also, the present invention provides such repair efficiency without the need for an excessive number of fuses which is characteristic of the Rountree repair system previously discussed.

**[0027]** As shown in FIG. 3, selection fuses 90 in a semiconductor memory 92 of the present invention may be programmed to output a block repair enable signal EN and fuse signals F(0:2) to select circuitry 94. When active, the block repair enable signal EN enables a block repair within an array 96 of the semiconductor memory 92 using a selected redundant row within the semiconductor memory 92. When inactive, the block repair enable signal EN enables conventional row repair within the array 96 using the selected redundant row. When block repair is enabled within the array 96, the status of the fuse signals F(0:2) determines the dimensions of the repaired block. Together, the fuse signals F(0:2) and the block repair enable signal EN may sometimes be referred to as a "block repair configuration."

**[0028]** It will be understood by those of ordinary skill in the art that only one enable signal EN and only one set of fuse signals F(0:2) are shown in FIG. 3 for purposes of clarity. In fact, redundant rows (*e.g.*, $\text{rrow}_0$, $\text{rrow}_1$, $\text{rrow}_2$, etc.) typically each have their own enable signal (*i.e.*, $EN_0$, $EN_1$, $EN_2$, etc.) and their own set of fuse signals (*i.e.*, $F_0(0:2)$, $F_1(0:2)$, $F_2(0:2)$, etc.) so that block repair or conventional repair can be selected for each redundant row using its enable signal, and so the dimensions of the repair block can be determined for each redundant row using its fuse signals if block repair is selected. For the purposes of this disclosure, rows and columns may be interchanged (*i.e.*, instead of a redundant row, a redundant column may be used).

**[0029]** Although the present invention will be described with respect to a 64 KB memory, it will be understood by those of ordinary skill in the art that the invention is applicable to any size memory. Additionally, for the purposes of this detailed description, rows and columns may be interchanged (*i.e.*, instead of a redundant row, a redundant column may be used.) It will also be understood that the invention is applicable to a wide variety of semiconductor memories, including, for example, magnetic random access memory (MRAM), dynamic RAM (DRAM), synchronous DRAM (SDRAM), double data rate SDRAM (DDR SDRAM), RAMBUS® DRAM (RDRAM®), extended data-out DRAM (EDO DRAM), fast-page-mode DRAM (FPM DRAM), static random access memory (SRAM), SyncBurst™ SRAM, Zero Bus Turnaround™ SRAM (ZBT™ SRAM), Quad Data Rate™ SRAM (QDR™ SRAM), DDR synchronous SRAM (DDR SRAM) and nonvolatile electrically block-erasable programmable read only memory (Flash). Further, it will be understood by those of ordinary skill in the art that any non-volatile element (*e.g.*, fuses, anti-fuses, or flash EEPROM cells) will work for purposes of the selection fuses 90, as will be explained in more detail below with respect to FIGS. 4A, 4B, and 4C.

**[0030]** Upon receiving the enable signal EN and the fuse signals F(0:2), the select circuitry 94 outputs selection signals S(0:7) as shown in Table 1 below.

Table 1

| EN | F2 | F1 | F0 | S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 | S(0:7) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 15 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 31 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 63 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 127 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 255 |

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Of course, it will be understood by one of ordinary skill in the art that although only one set of selection signals S(0:7) is discussed here, in fact each redundant row within the redundant array 98 typically has an associated set of selection signals S(0:7).

**[0031]** In response to the selection signals S(0:7), and upon receiving row address signals RA(0:7) during a memory operation, mux circuitry 100 outputs compare signals CMP(0:7) as shown in Table 2, below.

Table 2

| S(0:7) | CMP7 | CMP6 | CMP5 | CMP4 | CMP3 | CMP2 | CMP1 | CMP0 |
|---|---|---|---|---|---|---|---|---|
| 0 | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 |
| 1 | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | CA7 |
| 3 | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | CA6 | CA7 |
| 7 | RA7 | RA6 | RA5 | RA4 | RA3 | CA5 | CA6 | CA7 |
| 15 | RA7 | RA6 | RA5 | RA4 | CA4 | CA5 | CA6 | CA7 |
| 31 | RA7 | RA6 | RA5 | CA3 | CA4 | CA5 | CA6 | CA7 |
| 63 | RA7 | RA6 | CA2 | CA3 | CA4 | CA5 | CA6 | CA7 |
| 127 | RA7 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | CA7 |
| 255 | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | CA7 |

**[0032]** Thus, mux circuitry 100 passes the most significant bits of the row address RA(0:7) through in accordance with the selection signals S(0:7). As will be discussed below, this determines the "height" (*i.e.*, the number of rows spanned) of a repair block. Thus, for example, with the selection signals S(0:7) all set to zero, the repair block has the height of a single row (because all bits of the row address RA(0:7) are passed through as compare signals CMP(0:7)). This only occurs when the repair block enable signal EN is inactive, so that conventional row repair is enabled. If, instead, the selection signals S(0:7) are set to fifteen, for example, then the repair block is sixteen rows high (because the four most significant bits of the row address RA(0:7) are passed through the mux circuitry 100). Finally, if the selection signals S(0:7) are set to two-hundred fifty-five, for example, then the repair block is two-hundred fifty-six rows high (*i.e.*, the height of an entire column). Alternatively, the enable signal EN may be eliminated if one combination of fuse signals F(0:2) is used to decode the disable state (*i.e.*, F(0:2) all unprogrammed can represent block repair disable). Then one of the states of S(0:7) will not be available since there would only be seven remaining states of S(0:7) in the above example.

**[0033]** A portion of the address of a defective memory cell within the array 96 is stored using bad address storage fuses 102 and is output by the fuses 102 as bad address BA(0:7). If, for example, conventional row repair is being used to repair the defective memory cell, then the fuses 102 are programmed to output a bad address BA(0:7) equivalent to the row address of the defective cell. If, instead, a repair block sixteen rows high, for example, is being used to repair the defective cell, then the fuses 102 are programmed so the four most significant bits of the bad address (*i.e.*, BA7, BA6, BA5, and BA4) match the four most significant bits of the row address of the defective cell, and so the four least significant bits of the bad address (*i.e.*, BA3, BA2, BA1, and BA0) match the four most significant bits of the column address of the defective cell (for reasons that will be explained below). Finally, if the repair block used to repair the defective cell is an entire column within the array 96, then none of the fuses 102 are programmed with bits from the row address of the defective memory cell. Instead, the fuses 102 are programmed with the column address of the defective memory cell (again, for reasons that will be explained below).

**[0034]** Of course, it will be understood by one of ordinary skill in the art that each redundant row in the redundant array 98 typically has its own associated bad address BA(0:7). Only one is discussed here for purposes of clarity. Also, it will be understood that the fuses 102 may comprise any non-volatile element including, for example, fuses, anti-fuses, or flash EEPROM cells, as will be discussed below with respect to FIGS. 4A, 4B, and 4C.

**[0035]** The compare signals CMP(0:7) also include the column address CA(0:7) as shown in Table 2. The compare circuitry 104 compares the compare signals CMP(0:7) to the bad address BA(0:7). If there is no match, the column address CA(0:7) is used to select a column of the array 96. When a match occurs, a column is selected by a column decoder 110 in accordance with redundant decode signals DEC(0:7) that are output by the mux circuitry 100 as shown in Table 3, below.

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Table 3

| S(0:7) | DEC7 | DEC6 | DEC5 | DEC4 | DEC3 | DEC2 | DEC1 | DEC0 |
|---|---|---|---|---|---|---|---|---|
| 0 | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | CA7 |
| 1 | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | RA0 |
| 3 | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | RA1 | RA0 |
| 7 | CA0 | CA1 | CA2 | CA3 | CA4 | RA2 | RA1 | RA0 |
| 15 | CA0 | CA1 | CA2 | CA3 | RA3 | RA2 | RA1 | RA0 |
| 31 | CA0 | CA1 | CA2 | RA4 | RA3 | RA2 | RA1 | RA0 |
| 63 | CA0 | CA1 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 |
| 127 | CA0 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 |
| 255 | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 |

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**[0036]** The selection fuses 90 and the bad address storage fuses 102 of FIG. 3 may comprise any non-volatile elements including, for example, fuses 120 as shown in FIG. 4A, anti-fuses 122 as shown in FIG. 4B, and flash EEPROM cells 124 as shown in FIG. 4C.

**[0037]** As shown in FIG. 5, the select circuitry 94 of FIG. 3 includes a NOR gate 130, inverters 132, and NAND gates 134 for implementing the operations of the circuitry 94 as described above with respect to Table 1. Of course, it will be understood by one of ordinary skill in the art that any device for selecting the height and width of a repair block will work for purposes of the present invention, and that such a device need not necessarily include the circuitry shown in FIG. 5 or operate in accordance with Table 1.

**[0038]** As shown in FIG. 6, the mux circuitry 100 includes a plurality of mux circuits 140 for implementing the operations of the circuitry 100 as described above with respect to Tables 2, 3, and 4. Again, it should be understood that any device for routing the proper row and column addresses to the compare circuitry 104 (see FIG. 3) will work for purposes of the present invention, and that such a device need not necessarily operate in accordance with Tables 2 and 3.

**[0039]** It should be noted that, as described thus far, the present invention only uses repair blocks that stay within "logical" boundaries of the array 96 of FIG. 3. In addition, a repair block that spans one quarter of the rows in the top half of the array 96, for example, and one quarter of the rows in the bottom half can be implemented using an alternative embodiment described below.

**[0040]** In this embodiment, repair blocks that cross logical boundaries within the array 96 of FIG. 3 may be used. For example, a repair block that spans an odd number of rows in the top half of the array 96 and an even number of rows in the bottom half of the array 96 can be implemented using this embodiment. Such an embodiment typically requires that additional bad address storage fuses 102 (see FIG. 3) be provided to store additional bits from the row and column addresses of a defective memory cell. These additional bits are typically necessary to identify a match when row and column addresses are received. Such an embodiment also typically requires that the compare circuitry 104 (see FIG. 3) be constructed to perform the necessary logical operations to determine a match. This embodiment thus requires additional fuses or other non-volatile elements, but provides greater flexibility in selecting the optimum location of repair blocks.

**[0041]** In the specific example described, the row address Most Significant Bit (MSB) may be replaced with an XOR function of the MSB and the next lower row address term for the repair address match. Likewise, logical combinations of column address terms may be used in place of single column address terms to "shift" or split the repair block in the column dimension. For example, replacing the column MSB with an XAND function of the two most significant column address bits will split the repair block and match upper and lower quarters of the column address space rather than upper or lower halfs.

**[0042]** As shown in FIG. 7, the semiconductor memory 92 of FIG. 3 is fabricated on a semiconductor wafer 160. It should be understood that the semiconductor memory 92 may also be fabricated on a wide variety of other semiconductor substrates including, for example, a Silicon-On-Insulator (SOI) substrate, a Silicon-On-Glass (SOG) substrate, and a Silicon-On-Sapphire (SOS) substrate.

**[0043]** As shown in FIG. 8, an electronic system 170 includes an input device 172, an output device 174, a processor device 176, and a memory device 178 that incorporates the semiconductor memory 92 of FIG. 3. Of course, it should be understood that the semiconductor

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memory 92 may also be incorporated into any one of the input device 172, the output device 174, and the processor device 176.

**[0044]** Although the present invention has been described with reference to particular embodiments, the invention is not limited to these described embodiments. Rather, the invention is limited only by the appended claims, which include within their scope all equivalent devices or methods that operate according to the principles of the invention as described herein.

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